

FEATURES

Composite Video Output

Chrominance and Luminance (S-Video) Outputs

No External Filters or Delay Lines Required

Drives 75Ω Reverse-Terminated Loads

Compact 28-Pin PLCC

Logic Selectable NTSC or PAL Encoding Modes

Logic Selectable NTSC or PAL Encoding Modes Automatically Selects Proper Chrominance Filter

Automatically Selects Proper Chrominance Cutoff Frequency for Encoding Standard

Cutoff Frequency for Encoding Standard Logic Selectable Encode or Power-Down Mode (AD720)

Logic Selectable Encoding in Power-Down Mode (AD720 Only)

Logic Selectable Encoder

Logic Selectable Low Power 30

Low Power: 200mW typical

APPLICATIONS

PRODUCT DESCRIPTION

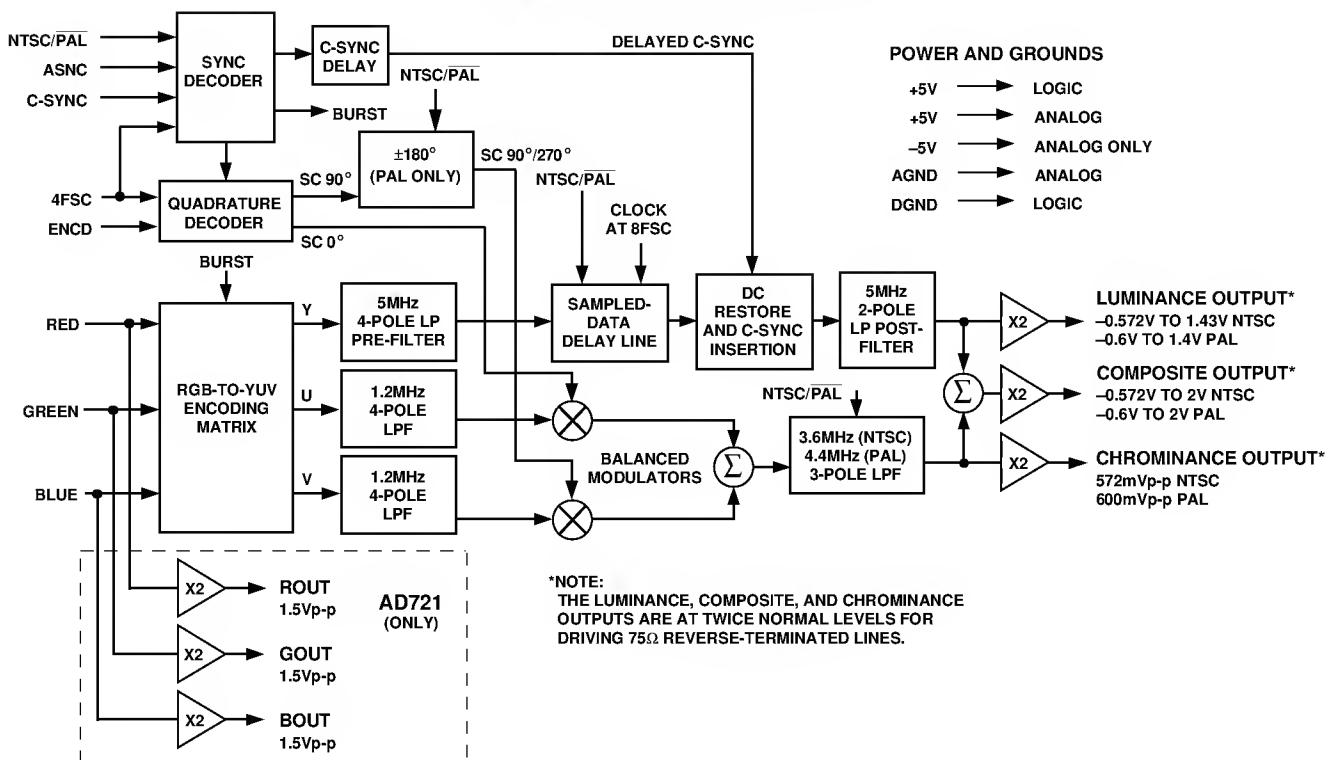
PRODUCT DESCRIPTION
The AD 720 and AD 721 RGB to NTSC/PAL Encoders convert red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance

(subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide a composite video output. All three outputs are available separately at voltages of twice the standard signal levels as required for driving $75\ \Omega$ reverse terminated cables. The AD 721 also features a bypass mode, in which the RGB inputs may bypass the encoder section of the IC via three gain-of-two amplifiers suitable for driving $75\ \Omega$ reverse terminated cables.

The AD 720 and AD 721 provide a complete, fully calibrated function, requiring only termination resistors, bypass capacitors, a clock input at four times the subcarrier frequency, and a composite sync pulse. There are two control inputs: one input selects the TV standard (NTSC/PAL) and the other (EN CD) powers down most sections of the chip when the encoding function is not in use (AD 720) or activates the triple bypass buffer to drive the RGB signals when RGB encoding is not required (AD 721). All logical inputs are CMOS compatible. The chip operates from +5 V supplies.

(continued on page 5)

FUNCTIONAL BLOCK DIAGRAM



REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

AD720/AD721- SPECIFICATIONS

($T_A = +25^\circ\text{C}$ and supplies = ± 5 V unless otherwise noted)

| Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------------------|------------------------------|---------------------------------------|------------|-----------|---------|
| SIGNAL INPUTS (RDIN, GRIN, BLIN) | | | | | |
| Input Amplitude | NTSC PAL | 714 700 | | | mV |
| Input Resistances ¹ | | | | | |
| RDIN with Respect to AGND | | 2.3 | | | kΩ |
| GRIN with Respect to AGND | | 4.2 | | | kΩ |
| BLIN with Respect to AGND | | 4.2 | | | kΩ |
| Input Capacitance | | 5 | | | pF |
| LOGIC INPUTS (C-SYNC, 4FSC, ENCD, NTSC) | | | | | |
| Logic LO Input Voltage | | | 1 | | V |
| Logic HI Input Voltage | | | 4 | | V |
| Logic LO Input Current (DC) | | <1 | | | μA |
| Logic HI Input Current (DC) | | <1 | | | μA |
| BYPASS AMPLIFIERS (AD721 Only) | | | | | |
| Gain Error | Nominal Gain of $\times 2^2$ | -5 100 -50 -50 | +5 | | % |
| Small Signal -3 dB Bandwidth | | 100 | | | MHz |
| Output Offset Voltage (Active State) | | +50 | | | mV |
| Output Voltage (Inactive State) | | +50 | | | mV |
| VIDEO OUTPUTS ³ (LUMA, CRM A, CMPS) | | | | | |
| Luminance (LUMA) Output | | | | | |
| Bandwidth | | 5 | | | MHz |
| Gain Error | | -5 | +5 | | % |
| Linearity | | ± 1 | | | % |
| Sync Level | NTSC PAL | ± 0.1 252 286 300 | 320 | | mV |
| Chrominance (CRM A) Output | | | | | |
| Bandwidth | NTSC PAL | 3.6 4.4 | | | MHz |
| Color Burst Amplitude | NTSC PAL | 286 300 | 315 | | mV p-p |
| Absolute Gain Error | | -15 | +15 | | mV p-p |
| Absolute Phase Error | | ± 5 ± 3 | | | % |
| Chroma/Luma Time Alignment ⁴ | NTSC | -170 | | | Degrees |
| Composite Output | | | | | ns |
| Absolute Gain Error | | -5 | +5 | | % |
| Differential Gain | | 0.1 | | | % |
| Differential Phase | | 0.1 | | | Degrees |
| Output Offset Voltage | | 50 | 100 | | mV |
| Chroma Feedthrough | MonoChrome Input | 20 | 55 | | mV p-p |
| POWER SUPPLIES (APOS, DPOS, VNEG) | | | | | |
| Recommended Supply Range | Dual Supply | ± 4.75 | ± 5.25 | | V |
| Full Output Current ⁵ | -5 V Supply | 35 | | | mA |
| | +5 V Supply | 67 | | | mA |
| Zero Signal Quiescent Current | -5 V Supply | 10 | 20 | 35 | mA |
| | +5 V Supply | 10 | 20 | 35 | mA |
| Bypass Mode Quiescent Current (AD721 Only) | -5 V Supply | | 14 | 20 | mA |
| | +5 V Supply | | 14 | 20 | mA |

NOTES

¹Input scaling resistors provide best scaling accuracy when source resistance is $37.5\ \Omega$ ($75\ \Omega$ reverse-terminated input).

²Required for driving a $75\ \Omega$ double reverse terminated load.

³All outputs are measured at a reverse-terminated load; voltages at IC pins are twice those specified here.

⁴This is a predistortion (per FCC specifications) that compensates for the chroma/luma delay in the low-pass filter that separates the luminance and chrominance signals in a television receiver.

⁵CRM A, LUMA, and CMPS outputs are all connected to $75\ \Omega$ reverse-terminated loads; full-white signal for entire field.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

| | |
|----------------------------------------------|-----------------|
| Supply Voltage $\pm V_S$ | ± 6 V |
| Internal Power Dissipation | 600 mW |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature, Soldering 60 sec | +300°C |

NOTE

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

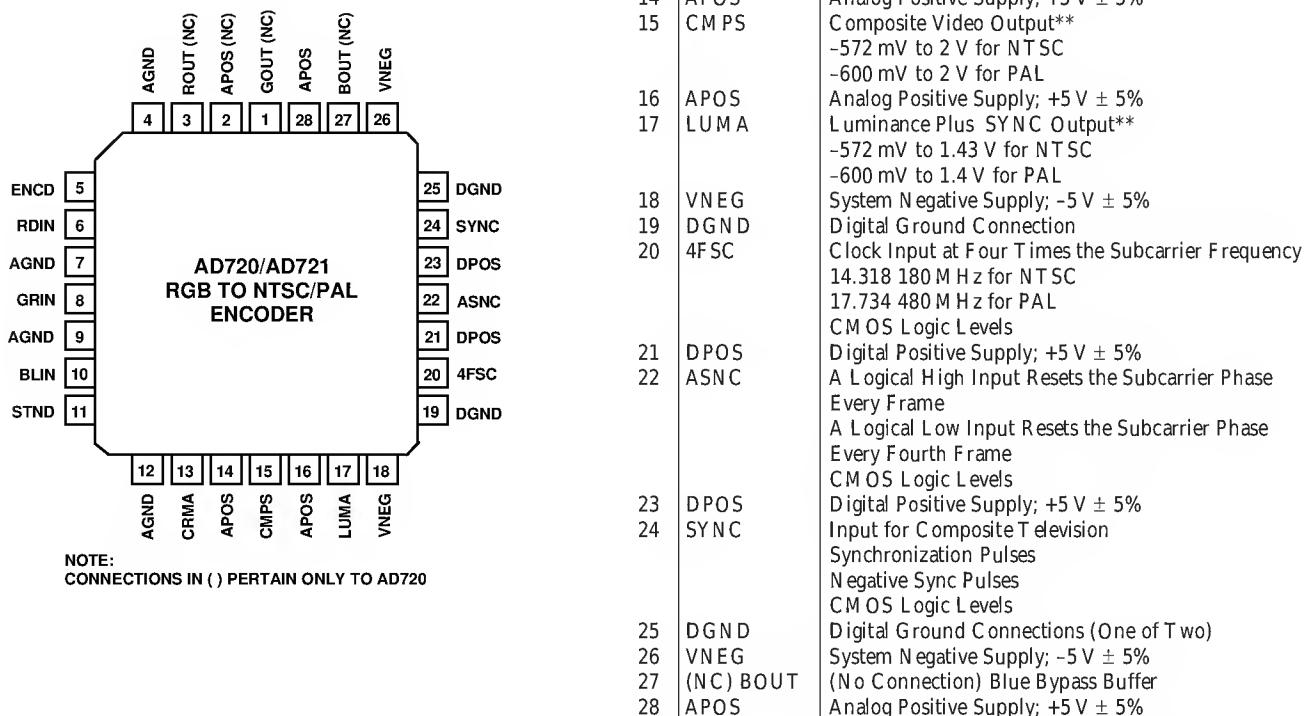
Thermal characteristics: 28-pin plastic package: $\theta_{JA} = 100^\circ\text{C}$.

ORDERING GUIDE

| Model | Temperature Range | Package | Package Option |
|----------|-------------------|-------------|----------------|
| AD 720JP | 0°C to +70°C | 28-Pin PLCC | P-28A |
| AD 721JP | 0°C to +70°C | 28-Pin PLCC | P-28A |

PIN CONNECTIONS

28-Lead Plastic Leaded Chip Carrier (PLCC) Package P-28A



NOTE:
CONNECTIONS IN () PERTAIN ONLY TO AD720

**() pertain only to AD 720.*

**The luminance, chrominance, and composite outputs are at twice normal levels for driving 75 Ω reverse-terminated lines.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD 720/AD 721 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD720/AD721- Typical Characteristics

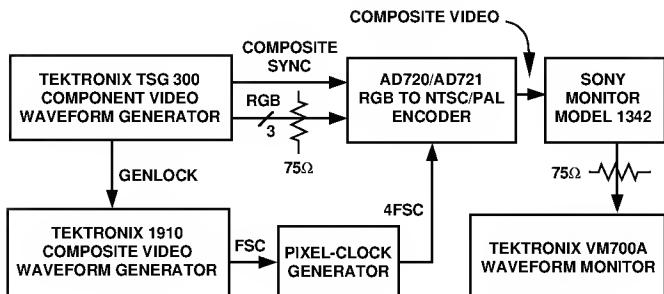


Figure 1. AD720/AD721 Evaluation Setup

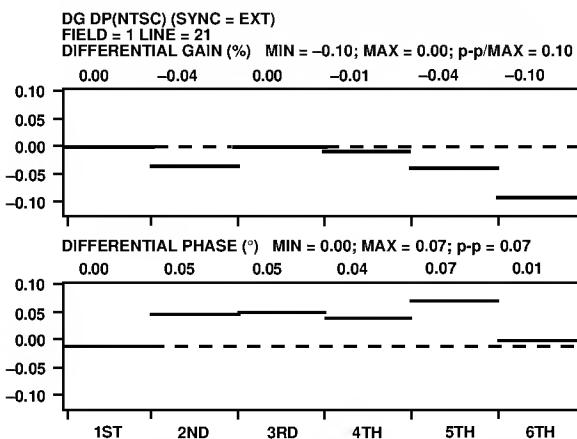


Figure 2. Composite Output Differential Phase and Gain, NTSC (Nulled to Chroma Output)

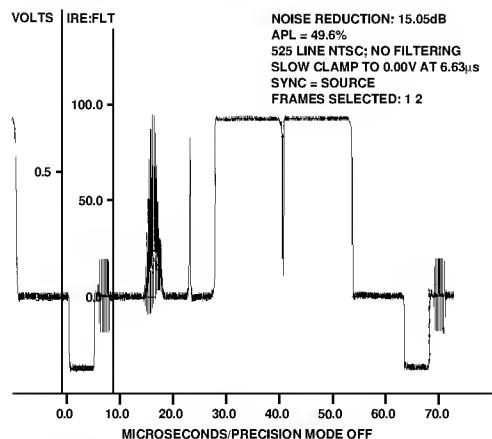


Figure 3. Modulated Pulse and Bar, NTSC

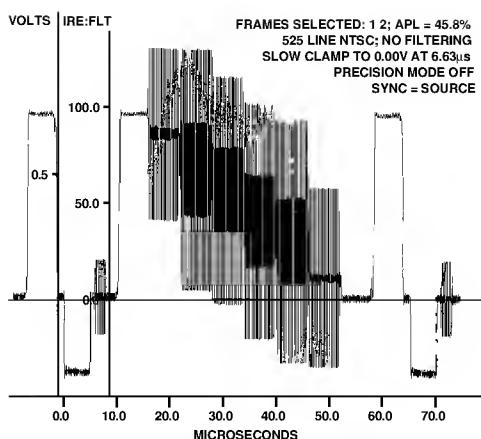


Figure 4. 100% Color Bars, NTSC

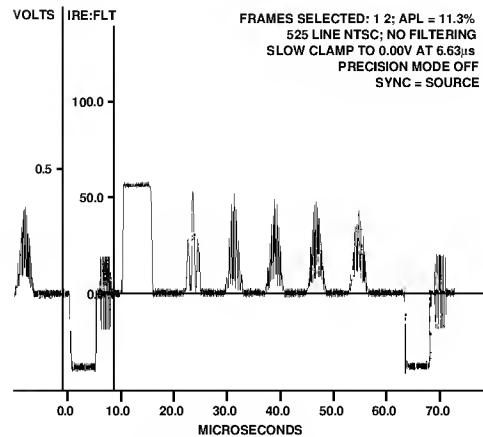


Figure 5. Multipulse, NTSC

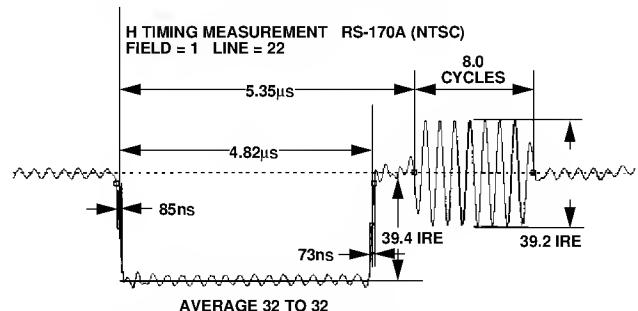


Figure 6. Horizontal Timing, NTSC

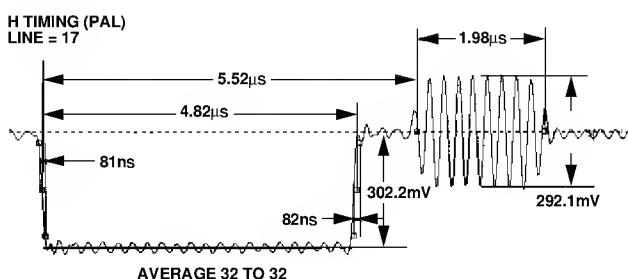


Figure 7. Horizontal Timing, PAL

(continued from page 1)

All required low-pass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip low-pass filters limit the bandwidth of the U and V color difference signals to 1.2 MHz prior to quadrature modulation of the color subcarrier; a third low-pass filter at 3.6 MHz (NTSC) or 4.4 MHz (PAL) follows the modulators to limit the harmonic content of the output.

Delays in the U and V chroma filters are matched by an on-chip sampled data delay line in the Y signal path; to prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a post filter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot. The overall delay is about 170 ns, which precompensates for delays in the filters used to decode the NTSC or PAL signal in a television receiver. (This precompensation delay is already present in TV broadcasts.)

The AD 720 and AD 721 are available in a 28-pin plastic leaded chip carrier for the 0°C to +70°C commercial temperature range.

THEORY OF OPERATION

Referring to the AD 720/AD 721 block diagram (Figure 8), the RGB inputs (each 0 mV to 714 mV in NTSC or 0 mV to 700 mV in PAL) are first encoded into luminance and color difference signals. The luminance signal is called the "Y" signal and the color-difference signals are called U and V. The RGB inputs are encoded into the YUV format using the transformation

$$Y = 0.299R + 0.587G + 0.114B$$

$$U = 0.493 (B-Y)$$

$$V = 0.877 (R-Y)$$

For NTSC operation, the chroma amplitude is increased by the factor 1.06 prior to summation with the luminance output. The burst signal is inserted into the Y channel in the encoding matrix.

The three outputs of the encoding matrix, now transformed into Y, U, and V components, take two paths. The Y (luminance) signal is passed through a delay line consisting of a prefilter, a sampled-data delay line, and a post filter. The pre- and post-filters prevent aliasing of harmonics back into the baseband video. The overall delay is a nominal -170 ns relative to the chrominance signal, in keeping with broadcast requirements to compensate for delays introduced by the filters in the decoding process.

The U and V components pass through 4-pole modified Bessel low-pass filters with a 1.2 MHz -3 dB frequency to prevent aliasing in the balanced modulators, where they modulate a 3.579 545 000 MHz (NTSC) or 4.433 618 750 MHz (PAL) signal via a pair of balanced modulators driven in quadrature by the color subcarrier.

The AD 720/AD 721 4FSC input drives a digital divide-by-4 circuit (two flip-flops) to create the quadrature signal. The reference phase 0° is used for the U signal. In the NTSC mode, the V signal is modulated at 90°, but in the PAL mode, the V modulation input alternates between 90° and 270° at half the line rate as required by the PAL standard. The outputs of the balanced modulators are summed and low-pass filtered to remove harmonics.

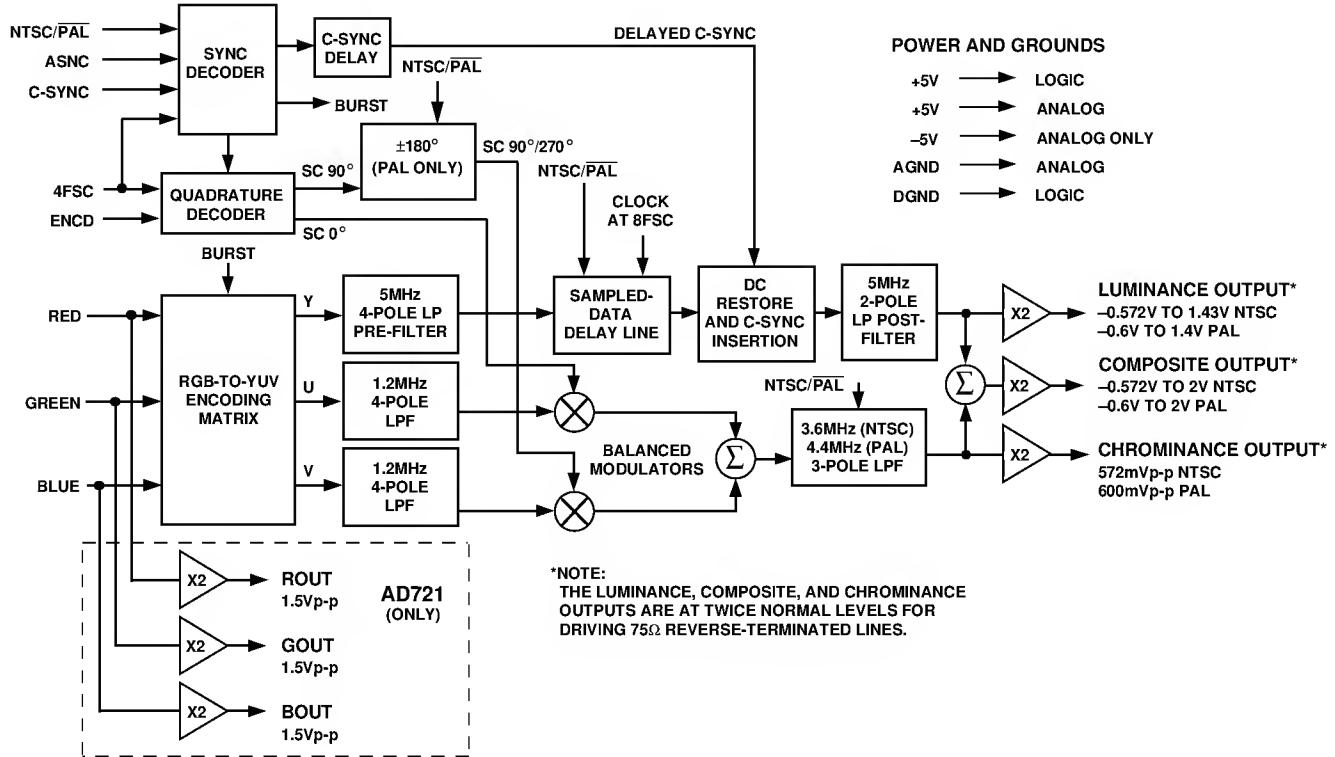


Figure 8. AD720/AD721 Functional Block Diagram

AD720/AD721

The filtered output is summed with the luminance signal to create a composite video signal. The separate luminance, chrominance, and composite video signals are amplified by gain-of-two amplifiers for driving $75\ \Omega$ reverse-terminated lines. The separate luminance and chrominance outputs together are known as "S-Video."

The digital section of the AD 720/AD 721 is clocked by the 4FSC input. It measures the width of pulses in the composite sync input to separate vertical, horizontal, and serration pulses and to insert the subcarrier burst only after a valid horizontal sync pulse.

Asserting the EN CD pin to a logical low routes the AD 721's RGB inputs through three gain-of-two bypass buffers for driving $75\ \Omega$ reverse-terminated lines, bypassing the encoder section of the AD 721. The triple bypass amplifier is utilized to overcome the loading effects of a "TV-out" connection on the RGB monitor output. When a video encoder is connected to outputs of a current-out video RAM DAC or VGA controller, the R, G, and B signals to the monitor are loaded-down. This requires the use of a gain block to properly drive the monitor.

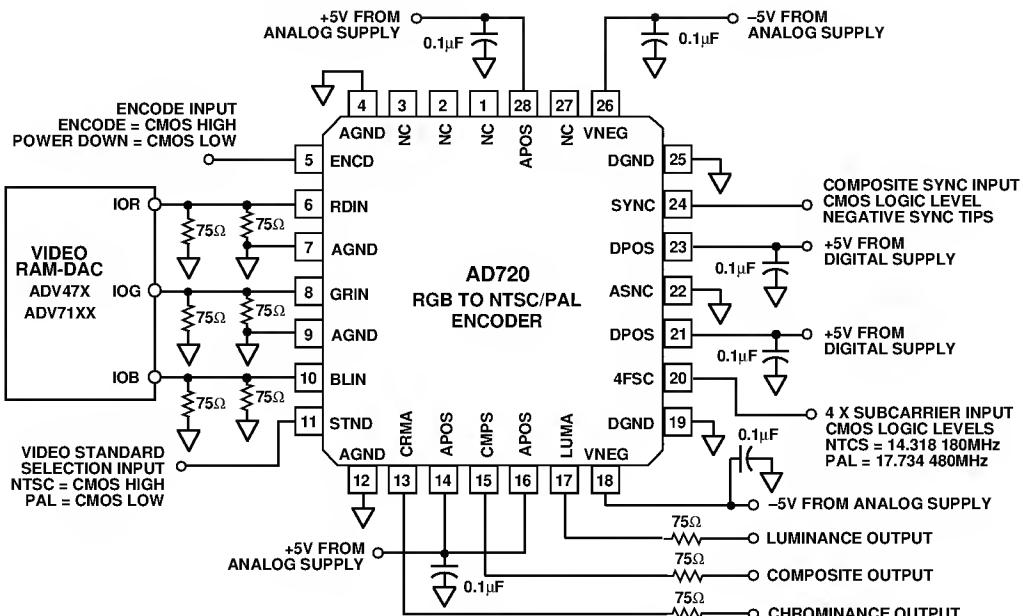


Figure 9. AD720 Application

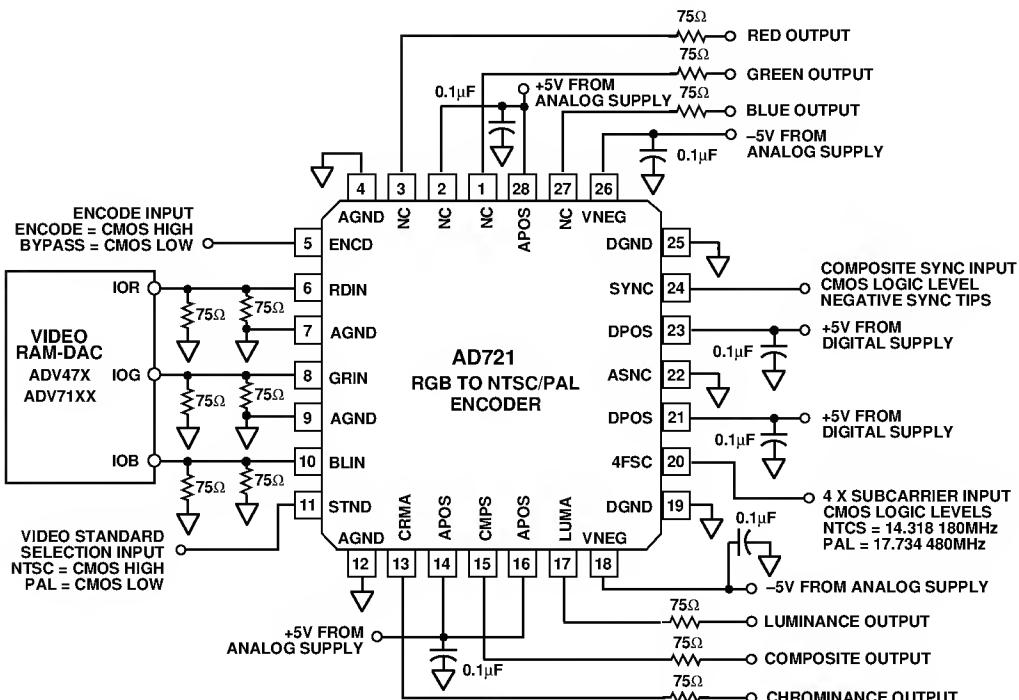


Figure 10. AD721 Application

APPLYING THE AD720/AD721

Figure 9 shows the application of the AD720 and Figure 10 shows the application of the AD721. Note that the AD720 and AD721 differ from other analog encoders because they are dc coupled. This means that, for example, the expected RGB inputs are 0 mV to 714 mV in NTSC and 0 mV to 700 mV in PAL. The luminance, chrominance, and composite outputs are also dc coupled. These outputs can drive a $75\ \Omega$ reverse-terminated load. Unused outputs should be terminated with $150\ \Omega$ resistors.

The RGB data must be supplied to the AD720/AD721 at NTSC or PAL rates, interlaced format. Various VGA chip set vendors support this mode of operation. Most computers supply RGB outputs in noninterlaced format at higher data rates than NTSC and PAL, which means that "outboard" encoders must supply some form of timing conversion before the RGB data reaches the AD720/AD721.

Note also that the AD720/AD721 does not have internal dc restoration and does not accept sync on green. The composite sync input is a separate, CMOS logical-level input and must be synchronized with the 4FSC input, which serves as the master clock for the AD720/AD721.

The AD720/AD721 does not implement two elements of the PAL and NTSC standards. In NTSC operation, it does not support the 7.5 IRE unit setup (1 IRE unit = 7.14 mV)—this must be added via software using the RGB inputs. Many RAM-DACs, such as the Analog Devices ADV471 and ADV478, offer a logic-selectable setup mode. In PAL operation, the AD720/AD721 does not implement a 25 Hz subcarrier offset.

Decoupling and Grounding

Referring to the pin descriptions, the AD720/AD721 uses multiple analog grounds, digital grounds, digital positive supply inputs, analog positive supply inputs, and analog negative supply inputs in order to maximize isolation between analog and digital signal paths.

The most sensitive input of the AD720/AD721 is the 4FSC pin: any noise on this pin directly affects the subcarrier and causes degradation of the picture. Digital and analog grounds should be kept separate and brought together at a single point.

All power supply pins should be decoupled using $0.1\ \mu\text{F}$ ceramic capacitors located as close to the AD720/AD721 as possible. In addition, ferrite beads may be slipped over the power supply leads to reduce high frequency noise.

If a high speed RAM-DAC is used (e.g., capable of 80 MHz operation with subnanosecond rise times), care must be taken to properly terminate the input printed-circuit-board traces to the AD720/AD721. Otherwise, ringing on these traces may occur and cause degradation of the picture.

APPLICATIONS HINTS

In applying the AD720/AD721, problems may arise due to incorrect input signals. A few common situations follow.

Fade to Black or White—Invalid Horizontal Sync Pulses

Some systems produce sync pulses that are longer or shorter than the NTSC and PAL standards specify. The digital sync

separator in the AD720/AD721 ignores horizontal sync pulses that are too long or too short. Figure 11 shows the timing windows for valid NTSC and PAL horizontal sync pulses.

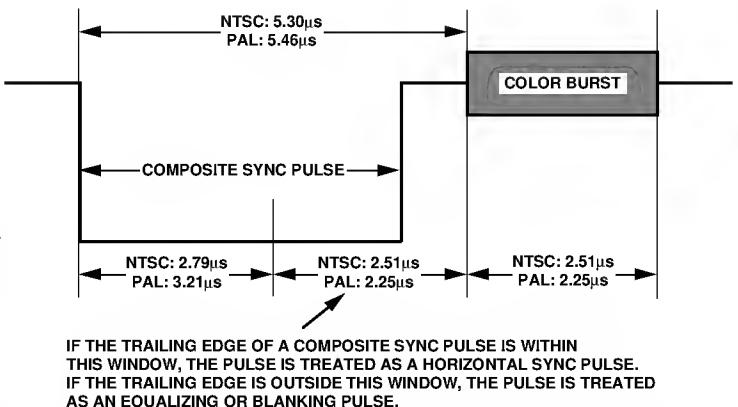


Figure 11. NTSC and PAL Timing for Valid Horizontal Sync Pulses

When the horizontal sync pulses are too long or too short, a dc offset voltage (due to charge storage) increases on the output of the sampled data delay line's auto-zero amplifier. Normally, this offset voltage is removed at the beginning of every line, as signified by the horizontal sync pulse. Without the horizontal sync pulse, the dc offset on the auto-zero amplifier increases over time (usually about three to five minutes) until it overrides the luminance information. The end result is a slow fade to black or white.

Color Flickering—Asynchronous Operation

The AD720/AD721 requires that its 4FSC and composite sync signals be synchronized. In most systems, when the two signals are synchronized, the composite sync signal is generated using a 4FSC signal as the reference. After every four frames, the AD720/AD721 resets the phase quadrature generator. When the CSYNC and 4FSC are synchronized, this reset is transparent to the system because the reference phase does not change. When the CSYNC and 4FSC are not synchronized, the difference between the reference phase and its new value upon reset causes an instantaneous color shift, which appears as a flickering in the color.

Adding NTSC Setup

The easiest way to add the 7.5 IRE unit¹ setup is to use a ADV471/478 or ADV477/475 or ADV473 type RAM-DAC, which have a logic-selectable setup (called "pedestal" on some data sheets and "setup" on others).

Color Fidelity

A source impedance other than $37.5\ \Omega$ ($75\ \Omega \parallel 75\ \Omega$ —a reverse-terminated $75\ \Omega$ input) can cause errors in the YUV encoding matrix, which is basically resistive and depends on the correct source impedance for accuracy. Figures 9 and 10 show the correct interface between a RAM-DAC and the AD720 and AD721 respectively, using $75\ \Omega$ reverse-terminated connections.

NOTE

¹IRE unit = 7.14 mV.

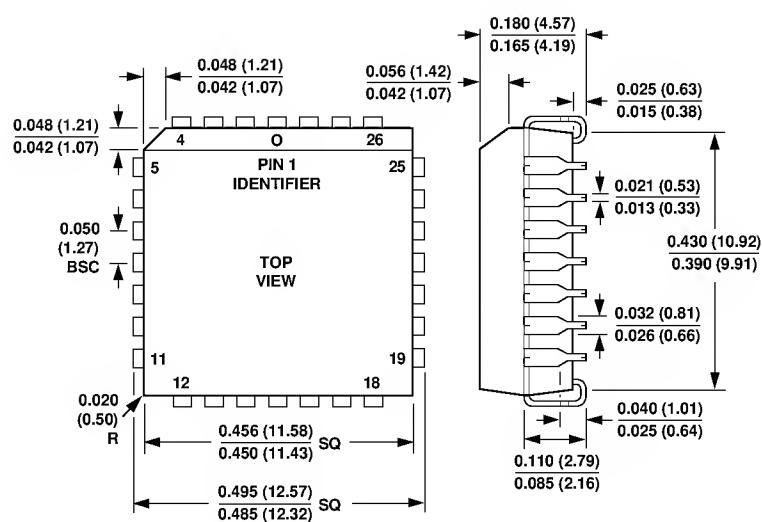
AD720/AD721

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Plastic Leaded Chip Carrier (PLCC) Package

P-28A



C1932-7.5-7/94

PRINTED IN U.S.A.